UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,816,731 B2
APPLICATION NO. : 12/321250
DATED : October 19, 2010
INVENTOR(S) : Parthasarathy et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specifications

Column 4, Lines 43-49 reads:

"In one embodiment, for a 2mm × 2mm die with 60µm high pillars, adequate stress relief is provided in a HVFET with an on-resistance of about 1 ohm utilizing a layout comprising four racetrack transistor sections separated by dummy silicon pillars, each having a pitch (y-direction) of about 13µm and a length (x-direction) of about 450µm."

It should read:

"In one embodiment, for a 2mm × 2mm die with 60µm high pillars, adequate stress relief is provided in a HVFET with an on-resistance of about 1 ohm utilizing a layout comprising four racetrack transistor sections separated by dummy silicon pillars, each having a pitch (x-direction) of about 13µm and a length (y-direction) of about 450µm."

Signed and Sealed this
Twenty-eighth Day of May, 2013

Teresa Stanek Rea

Teresa Stanek Rea
Acting Director of the United States Patent and Trademark Office